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| Дијаграм тока  микрооперација | Дијаграм тока  микрооперација | Секвенца управљачких сигнала |
| ADDR  ADDR  0  1 | ADDR  ADDR  0  1 | step00  br(if notADDR then step00) |
| 1  2  7  …  case(immed, memdir, memind, regind, regdir, predec, preinc) | 1  2  7  …  case(immed, memdir, memind, regind, regdir, predec, preinc) | step01  br(case(immed, memdir, memind, regind, regdir, predec, preinc) then (immed, step02), (memdir, step05), (memind, step06), (regind, step0B), (regdir, step0C), (predec, step0F), (preinc, step13) |
| ST  [1] immed  1  0 | ST  [1] immed  1  0 | step02  br(if ST then step1E) |
| JEQL  1  0 | JEQL  1  0 | step03  br(if JEQL then step1E) |
| B15..0 <= IR15..0  **EXEC** | ldB, mxB0  **EXEC** | step04  ldB, mxB0, br step1E |
| MAR15..0 <= IR15..0  [2] memdir  **READ** | ldMAR, mxMAR0  [2] memdir  **READ** | step05  ldMAR, mxMAR0, br step18 |
| MAR15..0 <= IR15..0  [3] memind | ldMAR, mxMAR0  [3] memind | step06  ldMAR, mxMAR0 |
| MDR7..0 <= MEM[MAR]  FCBUS  0  1 | ldMDR, rdMEM  FCBUS  0  1 | step07  ldMDR, rdMEM, br(if not FCBUS then step07) |
| B15..8 <= MDR7..0  MAR15..0 <= MAR15..0 + 1 | ldB15..8, incMAR | step08  ldB15..8, incMAR |
| MDR7..0 <= MEM[MAR]  FCBUS  0  1 | ldMDR, rdMEM  FCBUS  0  1 | step09  ldMDR, rdMEM, br(if not FCBUS then step09) |
| B7..0 <= MDR7..0 | ldB7..0 | step0A  ldB7..0 |
| MAR15..0 <= B15..0  **READ** | ldMAR, mxMAR1  **READ** | step0B  ldMAR, mxMAR1, br step18 |
| MAR15..0 <= R[IR19..16]  [4] regind  **READ** | ldMAR, mxMAR2  [4] regind  **READ** | step0C  ldMAR, mxMAR2, br step18 |
| ST  [5] regdir  1  0 | ST  [5] regdir  1  0 | step0D  br(if ST then step1E) |
| JEQL  1  0 | JEQL  1  0 | step0E  br(if JEQL then step1E) |
| B15..0 <= R[IR19..16]  **EXEC** | ldB, mxB1  **EXEC** | step0F  ldB, mxB1, br step1E |
| B15..0 <= R[IR19..16]  [6] predec | ldB, mxB1  [6] predec | step10  ldB, mxB1 |
| B15..0 <= B15..0 - 2 | decB | step11  decB |
| R[IR19..16] <= B15..0 | wrGPR, mxGPR | step12  wrGPR, mxGPR |
| MAR15..0 <= B15..0  **READ** | ldMAR, mxMAR1  **READ** | step13  ldMAR, mxMAR1, br step18 |
| B15..0 <= R[IR19..16]  [7] preinc | ldB, mxB1  [7] preinc | step14  ldB, mxB1 (R[IR19..16]15..0) |
| B15..0 <= B15..0 + 2 | incB | step15  incB |
| R[IR19..16] <= B15..0 | wrGPR, mxGPR | step16  wrGPR, mxGPR |
| MAR15..0 <= B15..0  **READ** | ldMAR, mxMAR1  **READ** | step17  ldMAR, mxMAR1 |
| ST  READ  1  0 | ST  READ  1  0 | step18  br(if ST then step1E) |
| JEQL  1  0 | JEQL  1  0 | step19  br(if JEQL then step1E) |
| MDR7..0 <= MEM[MAR]  FCBUS  0  1 | ldMDR, rdMEM  FCBUS  0  1 | step1A  ldMDR, rdMEM, br(if not FCBUS then step1A) |
| B15..8 <= MDR7..0  MAR15..0 <= MAR15..0 + 1 | ldB15..8, incMAR | step1B  ldB15..8, incMAR |
| MDR7..0 <= MEM[MAR]  FCBUS  0  1 | ldMDR, rdMEM  FCBUS  0  1 | step1C  ldMDR, rdMEM, br(if not FCBUS then step1C) |
| B7..0 <= MDR7..0  **EXEC** | ldB7..0  **EXEC** | step1D  ldB7..0 |
| ADDR <= 0, EXEC <= 1  EXEC  **ADDR** | clADDR, stEXEC  EXEC  **ADDR** | step1E  clADDR, stEXEC, br step00 |

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| Име и презиме | | Индекс | Потпис | Пројекат | |
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| Назив  Основи рачунарске технике 2 | | | | Датум | Страна |